What is claimed is:

1. An on-chip interconnect resistance and capacitance measurement structure, comprising:

a plurality of spatially adjacent interconnects;

a first circuit electrically connected to a first reference capacitor and a first interconnect of the plurality of interconnects;

a second circuit electrically connected to a second reference capacitor and the first circuit, the first and second circuits having a similar physical structure and an input, an output and two control terminals;

a first signal generator for driving the two circuits simultaneously through their input terminals;

a second signal generator for driving the two circuits through their two control terminals; and

a third signal generator for driving a second interconnect of the plurality of interconnects;

wherein the capacitance of the first interconnect is determined by measuring a current difference between the two circuits and the resistance of the second interconnect is determined by measuring a voltage drop between two positions having a known distance on the second interconnect when the third signal generator feeds a known current into the second interconnect.

2. The structure of claim 1, wherein the first and second reference capacitors are substantially similar to each other.

3. The structure of claim 2, wherein the first and second reference capacitors are two identical metal strips.

4. The structure of claim 1, wherein each of the two circuits comprises a PMOS transistor and an NMOS transistor that are electrically connected through their drain terminals to form a pseudo-inverter in which a source terminal of the PMOS transistor is said input terminal, a source terminal of the NMOS transistor is said output terminal and the two gate terminals are said two control terminals.

5. The structure of claim 4, wherein the second signal generator outputs two signals having a same frequency and first and second periods, a first of the two signals being fed into

the gate terminal of the PMOS transistor and a second of the two signals being fed into the gate terminal of the NMOS transistor.

6. The structure of claim 5, wherein the two signals are arranged such that no more than one of the two transistors in each pair conducts current at a given time, and the PMOS transistor is on and the NMOS transistor is off during the first period and PMOS transistor is off and the NMOS transistor is on during the second period.

7. The structure of claim 5, wherein the first period is long enough for the reference capacitors and the first interconnect to be fully charged and the second period is long enough for the reference capacitors and the first interconnect to be fully discharged.

8. The structure of claim 5, wherein there is a transition period between the first period and the second period, and both the PMOS and NMOS transistors are off during the transition period.

9. The structure of claim 1, wherein the third signal generator is off when the first and second signal generators are on.

10. The structure of claim 1, wherein the first and second signal generators are off when the third signal generator is on.

11. The structure of claim 10, wherein the third signal generator provides a constant direct current to the second interconnect and the resistance between the two positions on the second interconnect is determined according to Ohm's law.

12. The structure of claim 1, wherein the plurality of interconnects are made of copper.

13. The structure of claim 1, wherein the plurality of interconnects and the first and second circuits are fabricated on a testing wafer and the measured interconnect resistance and capacitance are used for estimating a transmission delay at any of the plurality of interconnects.

14. The structure of claim 1, wherein the plurality of interconnects and the first and second circuits are fabricated on a scribe line of a production wafer and the measured interconnect resistance and capacitance are used for monitoring process variation.